Power Minimization of a 433-MHz *LC* VCO for an Implantable Neural Recording System

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***Abstract*—This paper presents a new random-search based integrated inductor optimization algorithm. The algorithm provides the designer with valuable information about design tradeoffs. It is used to design an inductor to minimize power dissipation in an *LC* VCO. The measured results show that a 53:1 power savings can be achieved over VCOs using inductors optimized only for maximum *Q*. Six 433-MHz VCOs were fabricated and measured. The VCO using the optimal inductor design has a measured minimum power dissipation of 1.2 mW in a 0.5-µm three-metal CMOS process.**

I. Introduction

Power consumption is a troublesome issue in all wireless systems. In most cases, designers strive to reduce power consumption in order to maximize battery life and to minimize heat generation. In a fully-implantable wireless system satisfaction of these two concerns places extremely challenging constraints on wireless system design. All power that is generated by an implanted device must be dissipated into the surrounding tissues. It has been demonstrated that power levels on the order of 10 mW are sufficient to cause significant temperature increases in body tissues [1]. Prolonged temperature increases of 5°C can lead to cell death. This presents a major problem for forthcoming fully-implantable wireless neural recording systems [2]. Such systems consist of approximately 100 amplifiers, signal processing circuitry, power rectification circuitry, analog-to-digital converters, and a wireless transmitter, all of which must be operated on a ~10-mW power budget and be integrated onto a single die. This results in an undersized wireless transmitter power budget (~5 mW), within which even 'ultralow power' systems cannot operate (e.g., [3]). Therefore we must strive to minimize the power dissipation for every component of the wireless system.

In the sections that follow, we describe the design of a low-power fully-integrated *LC* VCO. In Section II we review the methods of minimizing power in *LC* VCOs, emphasizing the importance of maximizing the equivalent parallel resistance of the inductor. Next, in Section III we describe the algorithm used to design an optimal inductor with maximum parallel resistance. In Section IV we discuss the results of the optimization algorithm. We provide measured results of a fabricated VCO that uses the optimum inductor in Section V. Finally, in Section VI we offer some conclusions.

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II. Power Minimization Methods In *LC* VCOs

Figure 1 shows the standard *LC* VCO topology we have chosen. The dominant loss mechanism in the circuit is the series resistance of the spiral inductor. It has been demonstrated that losses in the MOS varactors are negligible due to their high quality factors [3, 4].

A. Maximization of R_p

The *LC* VCO in Fig. 1a can be modeled as a simple parallel *RLC* circuit, as illustrated in Fig. 1b. We lump all parasitic capacitances (i.e., C_p and C_s of the inductor and $C_{gsn,p}$, C_{gdp}, and $C_{dbn,p}$ for the transistors) and load capacitances into C. The equivalence of the series and parallel *RL* models for the inductor is valid only near the resonant frequency ω, and it can be shown that the

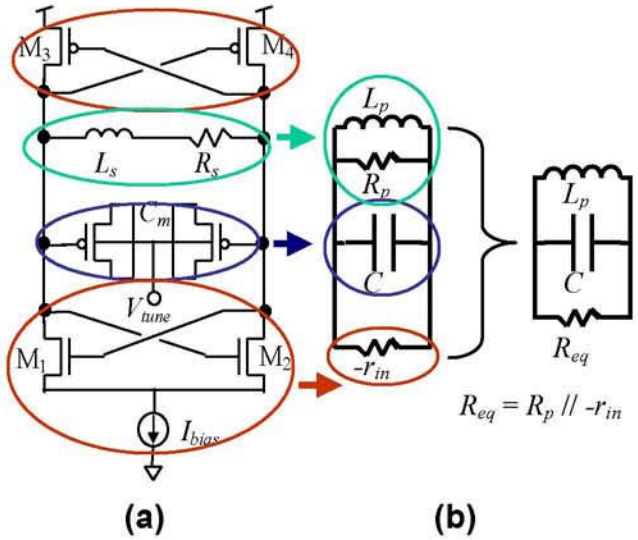

Figure 1. (a) *LC* VCO circuit. (b) Equivalent circuit.

components are related by

$$R_p = R_s\left(Q^2+1\right) \quad L_p = L_s\left(Q^2+1\right)/Q^2 \tag{1}$$

where Q is the quality factor of the inductor given by

$$Q = \omega L_s / R_s . \tag{2}$$

We do not use the definition of Q given in [5] because we employ a patterned ground shield (this has been shown to effectively eliminate the substrate loss factor), and the self-resonance factor is irrelevant when the inductor is placed in a tank circuit [5]. It can be shown that the input impedance of the cross-coupled devices is given by

$$-r_{in} = 1/g_m = 1/\sqrt{I_{bias}\mu_n C_{ox} W/L} \tag{3}$$

where g_m is the strong-inversion transconductance of the devices. If the devices are operated in moderate or weak inversion, g_m becomes linearly dependent on I_{bias}. We can see from Fig. 1b sustained oscillation is achieved when

$$R_{eq} \to -\infty \text{ i.e., } r_{in} = R_p. \tag{4}$$

The VCO power is proportional to I_{bias} and hence $1/R_p^2$ assuming strong-inversion operation, as can be seen from (3) and (4). Therefore, to minimize power we must maximize R_p.

B. Transistor Sizing

In addition to the dependence on I_{bias}, the incremental resistance of the cross-coupled transistors is also determined by the transistor aspect ratio W/L. Therefore, we can also reduce power consumption by increasing W/L. Also, we can omit a CMFB circuit and employ cross-coupled pMOS devices. However, these approaches have limitations: the transistor C_{gs} is directly proportional to W/L while r_{in} is inversely proportional to $\sqrt{W/L}$. As a result, the inductor self-resonant frequency (*SRF*) inductor and the VCO tuning range are reduced by choosing an excessively large W/L.

C. Supply Voltage Scaling

Perhaps the most popular method of reducing the power dissipation of any circuit is through supply voltage reduction. Indeed, VCO designs operating off of a 1-V supply have been reported (e.g., [3]). Unfortunately, the supply voltage in our application (an implantable neural recording system) is fixed at 3.3 V.

III. Inductor Optimization

Over the years several techniques have been proposed for optimizing the design of integrated inductors e.g., [6, 7]. While these methods produce well-optimized inductors, they do not necessarily provide the designer with information about design tradeoffs. In contrast, the algorithm described below allows the designer to investigate such tradeoffs easily.

A. Modeling Assumptions

We employ the lumped, symmetric inductor model given in [5]. Inductances are computed using the expressions given in [8]. Substrate losses are assumed to be negligible because patterned ground shields are used. However, we do account for eddy current resistance due to the conductive substrate with the approximation offered in [9]. The inter-turn spacing s for all inductors is fixed at 2.4 μm to satisfy design rules. We assume that the main part of the spiral is constructed by strapping together the top two layers of a three-metal process, the center tap is on the bottom metal layer, and the patterned ground shield is implemented in poly. Layer capacitance and resistivity information is taken from the MOSIS parametric data, averaged over several recent runs, for the AMI 0.5-μm CMOS process.

B. Algorithm Overview

In this work, we employ an empirical, brute force approach: a guided random search. Specifically, we generate a large number of inductors that cover the inductor design space, compute their lumped-model circuit parameters, and rank them according to some performance metric. The algorithm proceeds similarly to a genetic search, however ranking is done only on a per generation basis (i.e., ranking does not consider inductors from previous generations). As a result, the algorithm does not converge on a particular solution. Instead, it traverses the design space, keeping track of the best candidates from each region. After, the algorithm has been run for many generations, we apply the ranking to the top inductors from each generation to choose the optimum solution. Clearly this technique is less computationally efficient than other methods, but with today's high speed computers computational efficiency is less important as in the past. Furthermore, since we have a list of 'good' inductors from different areas in the design space, we can easily investigate tradeoffs.

C. Implementation Details

Each generation starts with the top 10 inductors from the previous generation. In the first generation, these 10 inductors are chosen randomly from the entire design space. For each of these 10 inductors, 180 new inductors are generated by randomly perturbing the design parameters (diameter d, turn width w, and number of turns n) by a small amount, excluding inductor geometries that are not physically realizable. Next, model parameters such as equivalent tank resistance R_p, quality factor Q, and self-resonance frequency *SRF* are computed for each inductor, and the maximum quantities for each generation are used compute normalized parameters. We then score the each inductor using a weighted average of their normalized parameters, pass the top 10 to the next generation, and place the top inductor into a 'best inductor' list. After the desired number of generations, we then apply the scoring/ranking to the inductors in the 'best inductor' list to determine the optimal inductor.

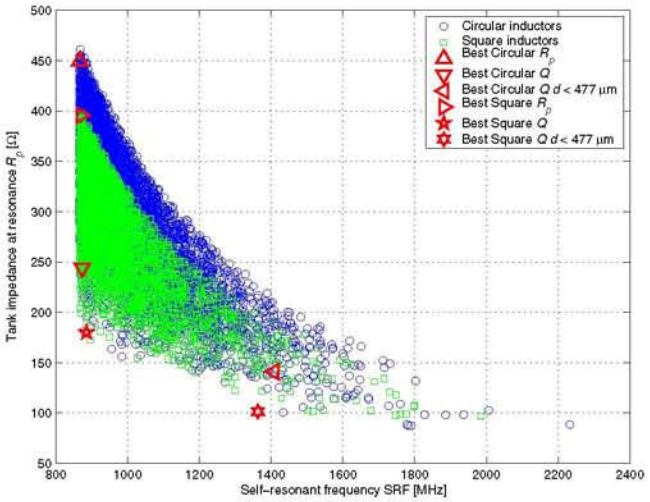

Figure 2. Tank resistance versus inductor self-resonant frequency.

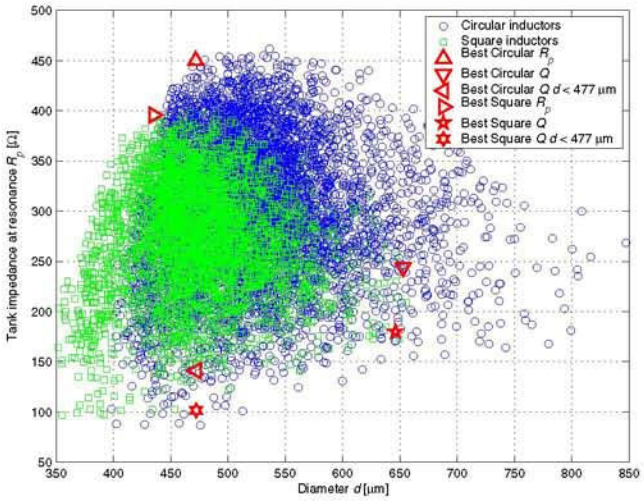

Figure 3. Tank resistance versus inductor diameter.

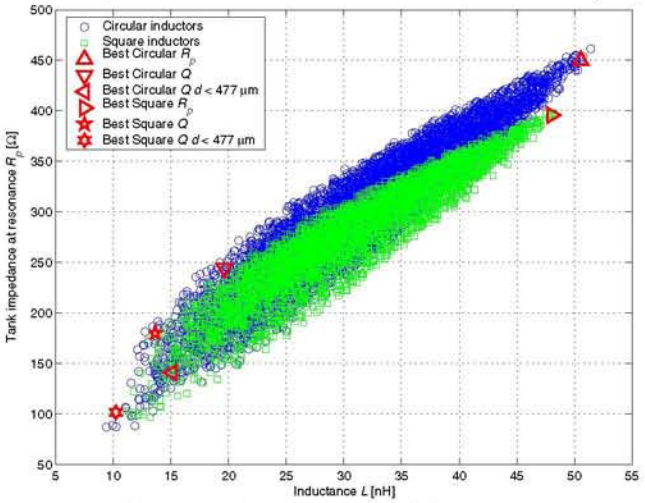

Figure 4. Tank resistance versus inductance.

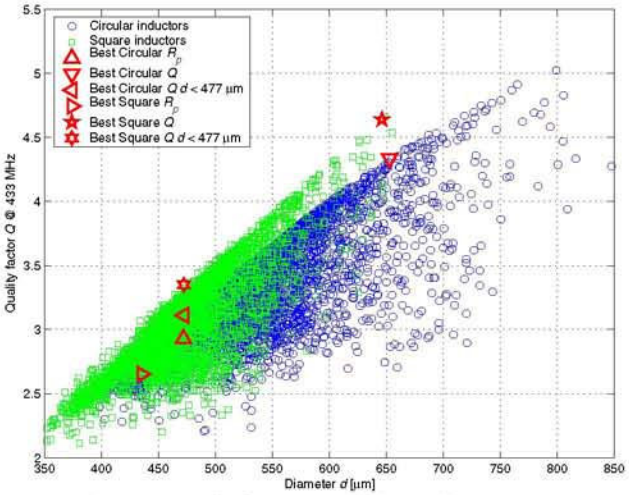

Figure 5. Quality factor versus inductor diameter.

In this work we considered square and circular geometries. The algorithm was run for 100,000 generations for both geometries. We based our score on R_p, Q, SRF, and inductor diameter with equal weighting for each parameter (the weighting for the diameter was negative to favor smaller inductors). Finally, we restricted the minimum allowable SRF to be twice the desired VCO frequency (433 MHz) to allow for an adequate tuning range and to limit frequency sensitivity due to poorly-controlled parasitic capacitances.

IV. Optimization Results

The results of our optimization procedure are shown in Figs 2-5. In all of the figures we have highlighted six inductors corresponding to three interesting optimization goals: 1.) maximize R_p and minimize diameter, d, 2.) maximize Q and minimize d,, and 3.) maximize Q and minimize d for $d <$ diameter of best inductor from goal (1). Square and circular geometries are considered separately. The parameters for these inductors are presented in Table I. The simulated VCO power corresponds to the 100-mVpp VCO output level.

We can observe from Figs 2-5 that the common wisdom promoting maximizing inductor Q does not necessarily lead to better inductors for low-power VCOs. Indeed, the best circular inductor has an R_p value 3.2 times larger (resulting in a VCO power dissipation 5 times lower) than the circular inductor with maximum Q and the same outside diameter. How can this observation be reconciled with (1) where it is clear that R_p is proportional to the square of Q? First, we note that the familiar goal of maximizing inductor Q relies on two premises: 1.) the inductance remains fixed, and 2.) Q varies widely. However, if we allow the inductance value to vary and we recognize that the range of Q factors available in integrated inductors is small (see Fig. 5), then our observation begins to make sense. To illustrate this point further, we can rewrite the expression for R_p in (1) as

$$R_p \approx QaL \tag{5}$$

which clearly illustrates that, for a fixed frequency ω, R_p is equally dependent on Q and L. Furthermore, we can see from Fig. 5 that the achievable range of Q is only one octave while Fig. 4 shows that L can vary over an entire decade.

TABLE I. INDUCTOR PARAMETERS

Inductor		Design Parameters					Model Parameters				VCO Power (mW)[1]	
Shape	*Optimization Goals*	*n*	*d (μm)*	*w (μm)*	*s (μm)*	*ρ (fill ratio)*	*L (nH)*	*R_p (Ω)*	*Q*	*SRF (MHz)*	*Simulated*	*Measured*
Circular	max R_p, min d	12.9	471.9	9.9	2.4	0.54	50.5	450	2.9	867	0.9	1.2
Circular	max Q, min d	8	652.8	29.7	2.4	0.74	19.6	244	4.3	874	1.9	5.6
Circular	max Q, min d for $d \leq 477$	8	472.2	20.1	2.4	0.70	15.1	141	3.1	1409	4.5	10.4
Square	max R_p, min d	10.9	435.3	9.9	2.4	0.44	48.0	396	2.7	870	1.0	1.5
Square	max Q, min d	5.8	646.2	42.6	2.4	0.67	13.6	180	4.6	886	3.0	19.4
Square	max Q, min d for $d \leq 477$	6	472.2	30.3	2.4	0.70	10.2	102	3.3	1363	8.4	63.8

[1] VDD = 3.3 V

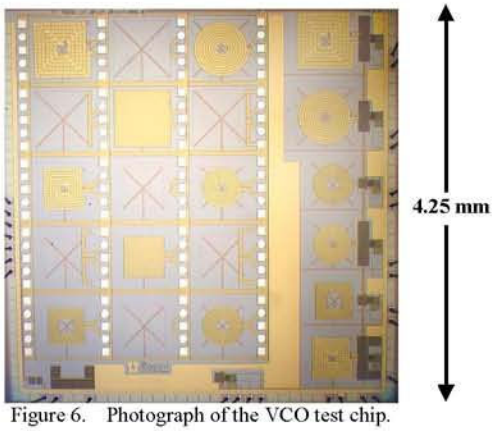

Figure 6. Photograph of the VCO test chip.

Finally, we note that circular geometry offers lower power operation than square, though the circular inductors must be slightly larger (see Fig. 3). Furthermore since square windings occupy more area than circular windings with the same outside diameter, the square inductors have larger parasitic capacitances and hence lower SRFs.

V. MEASURED RESULTS

We have fabricated VCOs using all six inductors in Table I (see Fig. 6). The power measurements for all VCOs are listed in Table I. The minimum power dissipation was measured to be 1.2 mW, in close agreement with the simulated value. This VCO has a 19% tuning range and phase noise of -100 dBc/Hz at a 600 kHz offset. The tuning range and phase noise measurements for the other VCOs are not yet available. Further measurements are also required to explain the discrepancy between the simulated and measured power dissipation. We believe that this discrepancy is due to optimistic predictions of R_p, but s-parameter measurements are required to confirm this suspicion.

VI. CONCLUSIONS

We have presented a new inductor optimization algorithm that provides the designer with valuable tradeoff information. We used this algorithm to design an optimized inductor for low-power VCO operation. Our results indicate that the conventional inductor optimization goal of simply maximizing Q does not necessarily lead to maximum tank resistance and hence minimum power dissipation for fully-integrated LC VCOs. Indeed, we have shown that maximizing R_p results in lower Q inductors. Interestingly, these inductors have as much as 53 times lower power dissipation than inductors optimized for maximum Q with the same outside diameter. Finally, we observed that circularly-shaped inductors can offer lower power dissipation than square-shaped inductors at the cost of a modest increase in diameter.

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